ABSTRACT OF THE DISCLOSURE

DLL circuit with a small minimum delay time while allowing a wide range of adjustment of the delay time. The DLL circuit according includes a first delay circuit for delaying an input clock signal (CLK1) to output a plurality of delayed clock signals (T_1 to T_N), a first selector (7) for selecting a first delayed clock signal (CLK_E) and a second delayed clock signal (CLK_O) from among the plurality of delayed clock signals (T_1 to T_N), for output, a second delay circuit (3) for delaying the input clock signal (CLK1) to generate a slightly delayed clock signal (CLKD), a second selector (4) for selecting two selected clock signals (FDLE, FDLO) from among the slightly delayed clock signal (CLKD), first delayed clock signal (CLK_E), and second delayed clock signal (CLK_O), and a delay synthesis circuit (5) for generating an internal clock signal (CLK_{IN}) from the selected clock signals (FDLE, FDLO), for output.